Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte MICHIO FUTAKUCHI

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Appeal No. 2000-0806
Application No. 09/016,398

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ON BRIEF

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Before FLEMING, LALL, and GROSS, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1-11, 13-23, and 25, the only claims pending in the application.

The invention relates to a ball grid array semiconductor integrated circuit device. A semiconductor chip (Specification, page 11, lines 1-2) having a plurality of connection pads is mounted to the first surface of a carrier base (Specification, page 11, lines 5-7). The connection pads connect to conductors (specification, page 11, line 14 to page 12, line 10) contained on and penetrating through the carrier base to the opposite surface, each connector connecting to one of a plurality of external connection terminals (Specification, page 12, lines 11-19) having a spherical shape. A sealing resin layer (Specification, page 12, lines 20-25) surrounds a periphery of the chip; in some embodiments, discrete first and second insulating adhesive layers (page 24, lines 1-10) are disposed below and above the chip, respectively. Along with the carrier base, a reinforcement base (page 12, line 26 to page 13, line 9) forms a "sandwich" of the core materials (chip, resin layer), the carrier base and reinforcement base having the same coefficient of thermal expansion whereby thermal stresses of the two bases in response to temperature change are substantially equal (page

14, lines 18-23).

In a further embodiment of the invention, the carrier base and reinforcement base have substantially the same size as the semiconductor chip (Specification, page 23, line 19 to page 25, line 3).

In a further embodiment of the invention, the semiconductor chip is not centrally located between the carrier base and the reinforcement base (Specification, page 20, lines 6-10), and the two bases have differences in at least one of modulus of elasticity and thickness (Specification, page 21, line 14 to page 22, line 11) such that, as a result, thermal stresses in the carrier base and the reinforcement base in response to temperature changes are substantially equal.

Independent claims 1, 14, and 23 are reproduced as follows:

1. A ball grid array semiconductor integrated circuit

device comprising:

a semiconductor chip having a plurality of connection pads;

a carrier base having a first surface to which the semiconductor chip is mounted;

a plurality of conductors, each conductor being electrically connected to a corresponding one of the connection pads; the conductors penetrating through the carrier base from the first surface to an opposite, second surface of the carrier base;

a plurality of external connection terminals, each external connection terminal having a spherical shape, being disposed on the second surface of the carrier base, and being electrically connected to a corresponding one of the conductors;

a sealing resin layer surrounding a periphery of the semiconductor chip; and

a reinforcement base, wherein the semiconductor chip and the sealing resin layer form a core material, the carrier base and the reinforcement base are skin materials sandwiching the core material, the semiconductor chip is located centrally between the carrier base and the reinforcement base, and the carrier base and the reinforcement base have the same coefficient of thermal expansion whereby thermal stresses in the carrier base and the reinforcement base in response to temperature changes are substantially equal.

14. A semiconductor integrated circuit device comprising:

a semiconductor chip having a plurality of connection pads;

a plurality of conductors, each conductor being

electrically connected to a corresponding one of the connection pads;

a plurality of external connection terminals, each connection terminal having a spherical shape and corresponding, respectively, to a corresponding one of the conductors;

a first insulating adhesive layer;

a second insulating adhesive layer;

a carrier base adhered to the semiconductor chip by the first insulating adhesive layer; and

a reinforcement base adhered to the semiconductor chip by the second insulating adhesive layer, wherein the semiconductor chip, the first insulating adhesive layer, and the second insulating adhesive layer form a core material, the carrier base and the reinforcement base have substantially the same size as the semiconductor chip and are skin materials, sandwiching the core material, the connections of the conductors to the connection pads are located at a first surface of the carrier base, the conductors are located in the carrier base, and

the external connection terminals are located at a second surface of the carrier base opposite the first surface.

23. A ball grid array semiconductor integrated circuit device comprising:

a semiconductor chip having a plurality of connection pads;

a plurality of conductors, each conductor being electrically connected to a corresponding one of the connection pads;

a plurality of external connection terminals, each

external connection terminal having a spherical shape and being electrically connected to a corresponding one of to the conductors;

a sealing resin layer surrounding a periphery of the semiconductor chip;

a carrier base having a first surface to which the semiconductor chip is mounted; and

a reinforcement base, wherein the semiconductor chip and the sealing resin layer form a core material, the carrier base and the reinforcement base are skin materials sandwiching the core material, the conductors being located at least partly in the carrier base, the external connection terminals being located at a second surface, opposite the first surface, of the carrier base, the semiconductor chip is not located centrally between the carrier base and the reinforcement base, and the carrier base and the reinforcement base have differences in at least one of modulus of elasticity and thickness so that, as a result of the differences, thermal stresses in the carrier base and the reinforcement base in response to temperature changes are substantially equal.

The Examiner relies on the following references:

Selna	5,640,048	Jun. 17, 1997
Suzuki	5,650,918	Jul. 22, 1997
Yamashita et al. (Yamashita)	5,726,493	Mar. 10, 1998
Dordi	5,835,355	Nov. 10, 1998

Claims 1, 4, 9-11, 13, 14, 16, 17, and 19-22 stand rejected under 35 U.S.C. § 103 as being unpatentable over

Dordi in view of Selna.

Claims 2, 5, 6, 8, 15, 18, 23, and 25 stand rejected under 35 U.S.C. § 103 as being unpatentable over Dordi, Selna, and Yamashita.

Claim 3 stands rejected under 35 U.S.C. § 103 as being unpatentable over Dordi, Selna, and Suzuki.

Claim 7 stands rejected under 35 U.S.C. § 103 as being unpatentable over Dordi, Selna, Suzuki, and Yamashita.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the brief and the answer for the details thereof.

OPINION

We will not sustain the rejection of claims 1-11, 13-23, and 25 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found
in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

On pages 8-15 of the Brief, Appellant argues that the Dordi reference applied by the Examiner does not teach a printed circuit board having vias within it and solder balls

on the opposite side of the printed circuit board for making connections; and that while the Selna reference does teach a printed circuit board having vias and opposite-mounted solder balls, no basis is suggested by the Examiner for combining the two references. Appellant further asserts that neither Dordi nor

Selna teaches a carrier base and reinforcement base having the same coefficient of thermal expansion; while admitting that Dordi discloses such a concept in its discussion of the prior art, Appellant asserts that there is no support in Dordi for the proposition that matching coefficients of thermal expansion of materials on opposite sides of a semiconductor chip in a ball grid array package is known or suggested in the prior art. Appellant further asserts that there is no element in Dordi that corresponds to the carrier base claimed, and that there is no element in Selna that corresponds to the reinforcement base. Further, Appellant asserts, even assuming the combination of Dordi and Selna teaches every element of the claimed invention, the person having ordinary skill in the art would not have found it obvious to make the combination advanced by the Examiner.

In the Answer, the Examiner admits that Dordi does not suggest vias in its printed circuit board, but asserts that Dordi's silence with regard to the use of vias does not rule out their use, and that it is "common practice" to use vias. The Examiner points to Selna for a teaching of vias in a printed circuit board as "an obvious extension to the Dordi device." The Examiner asserts[1] that it would be "simple" to substitute a printed circuit board with vias for another board lacking them. The Examiner admits that Dordi teaches matching coefficients of thermal expansion within a discussion of the prior art, but insists that such teaching is fully applicable against the instant invention. The Examiner further asserts that Figure 6 of Dordi illustrates a carrier base and reinforcement base being substantially the same size as the semiconductor chip.

As pointed out by our reviewing court, we must first

[1] We note that the Examiner's reference to Appellant's argument here as "[n]onsense" is inconsistent with the spirit of 37 CFR § 1.3, which requires applicants and their attorneys to conduct themselves with decorum and courtesy. MPEP § 707.07(d) cautions Examiners that "[e]verything of a personal nature must be avoided" in Office communications.

determine the scope of the claim. "[T]he name of the game is the claim." ***In re Hiniker Co.***, 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998).

Appellant's claim 14 recites a semiconductor integrated circuit device comprising a semiconductor chip having a plurality of connection pads, each connected on a first surface of a carrier base to a corresponding conductor, each conductor connected to a corresponding spherical-shaped external connection terminal on a second, opposite side of the carrier base, a first insulating adhesive layer adhering the carrier base to the semiconductor chip, a second insulating adhesive layer adhering a reinforcement base to the semiconductor chip, the carrier base and reinforcement base forming a "sandwich" with the insulating layers and semiconductor chip between them, and wherein the carrier base and reinforcement base have substantially the same size as the semiconductor chip.

We agree with the Examiner that Dordi teaches, as

noted *supra*, the semiconductor chip and associated connection pads and conductors; the carrier base (32); and the reinforcement base (34), the two bases being substantially the same size (see Fig. 6). Dordi teaches a first and second insulating adhesive layer (the sealing resin layer 36 below and above the semiconductor chip, respectively), the reinforcement base adhered to the semiconductor chip by the second insulating layer. Neither Dordi nor Selna, however, teach or suggest that the carrier base and reinforcement base have substantially the same size as the semiconductor chip. The Examiner argues that Dordi teaches this element, and points to Figure 6 for support of his position. As noted *supra*, Figure 6 does illustrate that stiffener 34, which corresponds to the reinforcement base of the instant invention, has substantially the same dimensions as tape 16, on which semiconductor chip 12 is mounted. Carrier base 32 is not illustrated in Figure 6; Dordi implies but does not explicitly teach that the carrier base has substantially the same size as the reinforcement base, by explaining that solder balls 26 align with and may be soldered to appropriate pads on

printed circuit board 32. Assuming that board 32 is appropriately sized to meet the claim language, however, Figure 6 clearly illustrates that semiconductor chip 12 does not have substantially the same size as reinforcement base 34. In Figure 6 of Dordi, semiconductor chip 12 is pictured as a rectangle at the center of a much larger rectangle depicting stiffener 34. Selna contains no teaching to remedy the deficiencies of Dordi; in all embodiments shown in Selna, semiconductor chip 12 is much smaller than the board to which it is mounted. Because the combination advanced by the Examiner does not contain every element of the claimed invention, we cannot sustain the rejection of claims 14-20 under 35 U.S.C.
§ 103.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84

n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore & Assocs.***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

Appellant's claim 1 recites a semiconductor chip having a plurality of connection pads; a carrier base having a first surface to which the chip is mounted; a plurality of conductors, each connected to a corresponding connection pad, penetrating through the carrier base to the opposite, second surface of the carrier base; a plurality of spherical-shaped external connection terminals disposed on the second surface of the carrier base, each electrically connected to a corresponding conductor; a sealing resin layer surrounding a periphery of the chip; and a reinforcement base, which along with the carrier base sandwiches the semiconductor chip and its associated resin layer, having the same coefficient of thermal expansion as the carrier base, such

that thermal stresses on the two bases in response to temperature changes are substantially equal.

Upon a careful review of Dordi and Selna, we fail to find any suggestion or reason to modify Dordi to use the printed circuit board of Selna as the "carrier base" of Appellant's invention. We agree with the Examiner that Dordi teaches a semiconductor chip (12) having a plurality of connection pads, surrounded by a resin layer (36). Dordi teaches that the chip is mounted on a thin tape (16, 16') rather than a printed circuit board or carrier base; Dordi further teaches a plurality of conductors (24, Fig. 1) that penetrate through the tape to an opposite surface, where each conductor connects to a spherical shaped connection terminal (26). Contrary to the assertions of both the Examiner and Appellant, Dordi explicitly teaches, within the detailed description of his invention, a stiffener (34) having a coefficient of thermal expansion (CTE) matching the coefficient of thermal expansion of the printed circuit board (32)(col. 5, lines 7-10). The difficulty in relying on Dordi, from the Examiner's point of view, is that if tape 16 is

construed to meet the limitation of a carrier base, such base does not have a CTE matching that of the reinforcement base; and that if printed circuit board 32 is construed to meet the limitation of a carrier base, such base does not have conductors penetrating through it to an opposite second surface containing external connection terminals.

The Examiner relies on Selna for a teaching of a printed circuit board structure having vias connected to external connection terminals on the opposite side of the board (column 5, line 50 to column 6, line 9). As mentioned *supra*, the Examiner argues that it would have been obvious to combine Dordi and Selna because "it is common practice to provide vias in PCBs . . . to allow the PCB to be connected to another PCB," and because "Selna shows just this feature and it makes an obvious extension to the Dordi device." The Examiner fails to point to any evidence, whether contained in Dordi, Selna, or any other prior art reference, that would have motivated the person having ordinary skill in the art to replace the PCB of Dordi with that in Selna containing the

desired vias. In the absence of evidence suggesting why the skilled artisan would have found it obvious to modify the invention of Dordi, having a PCB with no vias or connection terminals on its lower surface, to include such vias and connection terminals, we will not sustain the rejection of claims 1-11, 13, 21, and 22 under 35 U.S.C. § 103.

Appellant's claim 23 recites a ball grid array semiconductor integrated circuit device, including many limitations very similar to those contained in claim 1: a semiconductor chip, plurality of conductors, plurality of external connection terminals, a sealing resin layer surrounding the chip, a carrier base to which the chip is mounted, and a reinforcement base. The notable differences between claim 1 and claim 23 are that (a) the semiconductor chip is not mounted centrally between the carrier base and reinforcement base, and (b) rather than having matching coefficients of thermal expansion, the two bases have differences in at least one of modulus of elasticity and thickness, so that thermal stresses on the two bases in response to temperature changes are

substantially equal (notably, the same goal expressed in claim 1, and solved by matching CTEs).

The Examiner relies on a combination of Dordi, Selna, and Yamashita to arrive at the invention recited in claim 23. To meet the limitations first presented in claim 23 (chip location, base characteristics), the Examiner asserts that Yamashita teaches non-central location of the semiconductor chip, and two bases having different thicknesses, concluding that Yamashita "show a device which is simpler to fabricate than the Dordi device and it would have been obvious to employ it." We agree with the Examiner that Yamashita teaches, in two of its embodiments, an "intermediate plate 31" and a "heat release member 41" located at roughly the same spot as the reinforcement base of the instant invention; we further agree that the semiconductor chip 12 of Yamashita is not located centrally between printed circuit base 11 and the opposing plate/member. Yamashita, however, does not teach varying the modulus or thickness <u>in order to equalize thermal stresses</u> on the carrier base and reinforcement base. Yamashita teaches that intermediate plate

31 increases the available electrode pattern area, with improved inductance characteristics (column 8, lines 8-13). Yamashita teaches that the heat release member is meant to radiate excess heat away from the semiconductor chip and associated wiring (column 9, lines 18-23). Yamashita does not teach or suggest that thermal stresses on the printed circuit board and any "reinforcement base" are of concern, or that the modulus of elasticity or thickness of either board or base should be varied in order to make those stresses substantially equal. Even if we assume that Yamashita provided the intermediate plate and/or heat release member with a modulus of elasticity or thickness different from its printed circuit board, for the purpose of equalizing thermal stresses, the Examiner has presented no suggestion from the art of record as to why it would have been obvious to modify the Dordi invention, with its two bases having equal coefficients of thermal expansion, to use the "unequal" bases of Yamashita.

As noted *supra*, Dordi teaches a carrier base and reinforcement base having equal coefficients of thermal

expansion, presumably to achieve the same goals advanced by Appellant. Dordi, however, does not teach or suggest varying the modulus of elasticity or thickness of one of its bases in order to make the thermal stresses in the two bases in response to temperature changes substantially equal. In any event, the Examiner did not rely on Dordi to meet this limitation of Appellant's invention.

Upon a review of the references relied upon by the Examiner, we fail to find any suggestion or reason to provide a carrier base and reinforcement base having substantially the same size as the semiconductor chip, as recited in claim 14. Dordi and Selna teach semiconductor chips substantially smaller than the bases(s) on which they are mounted. Yamashita and Suzuki were not relied upon by the Examiner to teach sizing the bases as claimed, and in any case do not teach or suggest bases of an appropriate size. Therefore, we will not sustain the rejection of claims 14-20 under 35 U.S.C. § 103 as being unpatentable over Dordi and Selna.

In view of the foregoing, the decision of the Examiner rejecting claims 1-11, 13-23 and 25 under 35 U.S.C. § 103 is reversed.

REVERSED

MICHAEL R. FLEMING Administrative Patent Judge	)
PARSHOTAM S. LALL Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)

MRF:lbg

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